Remarks

The Office Action mailed April 30, 2004, and made final, has been carefully reviewed and the foregoing amendment has been made in consequence thereof.

Claims 1-19 are now pending in this application. Claims 1-19 stand rejected.

Applicants note the objections to the drawings. Applicants will submit formal drawings which address the issues noted in the Draftperson's Patent Drawing Review. For the reasons set forth above, Applicants request that the objections to the drawings be withdrawn.

The rejection of Claim 1 under 35 U.S.C. § 103 as being unpatentable over Robinson (U.S. Patent 5,708,838) in view of Robinson (U.S. Patent 6,567,837) is respectfully traversed.

Robinson '838 describes a system 100 which includes a host processor 102, and a plurality of object oriented processors 104, 106, 108 which are coupled to host processor 102 via a Comms bus 110. Each of the object oriented processors 104, 106, 108 includes a Comms interface 104a, 106a, 108a, an intelligent message handler 104b, 106b, 108b, and a hardware (peripheral) interface 104c, 106c, 108c. Each object oriented processor 104, 106, 108 is bi-directionally coupled via its respective Comms interface 104a, 106a, 108a to the Comms bus 110 which is coupled to host processor 102. High level messages sent by host processor 102, as instructed by the host software 103, are interpreted by the respective intelligent message handlers 104b, 106b, 108b and used to control the respective hardware interfaces 104c, 106c, 108c to control peripheral devices. Similarly, data from the peripheral devices are received by the respective hardware interfaces 104c, 106c, 108c, interpreted by the respective intelligent message handlers 104b, 106b, 108b and transmitted to the host as high level messages. Column 7, lines 35-60.

The high level command messages described from Column 8, line 40 to Column 10, , line 50 are not fairly characterized as an application program interface module defining a

programming interface for a class processor. Rather, the high level command messages are best characterized as a single programming interface where individual class processors and functions are addressed at specific portion of the message.

With regard to memory and memory allocation, Robinson '837 describes that an instantiation layer of the object calls a memory manager 38 and requests an allocation of RAM 14. The memory manager checks for the availability of RAM at 220 and if insufficient memory is available, sends an error message at 214. If enough RAM is available, the memory manager 38 returns a pointer to a starting address in RAM to the instantiation layer which receives the pointer and arranges its memory at 224. The memory manager also increments at 222 a heap pointer which is used by the memory manager to determine at 220 whether sufficient RAM is available for other instantiations. After the instantiation layer 46 successfully completes instantiation, it informs the system object 22 that instantiation was successful and sends the pointer to the system object at 226. When an object is instantiated, the instantiation layer arranges (at 224) its allocated RAM into organized parts. Column 10, lines 10-30. However, Robinson '837 does not describe a private localized read/write memory

Claim 1 recites a distributed processing system that comprises "a host processor including a host communication infrastructure (HCI) configured to provide communication with said host processor," "a plurality of class processors each having an associated private localized read/write memory" and "a plurality of application program interface modules each configured to provide an interface between said host communication infrastructure and at least one said class processor, said application program interface modules each defining a programming interface for a respective said class processor, wherein each said class processor responds to selected data messages on said HCI to perform selected computations utilizing said read/write memory."

Robinson '838 in view of Robinson '837 do not describe nor suggest such a system. Specifically, Robinson '838 in view of Robinson '837 do not describe nor suggest a plurality of application program interface modules each defining a programming interface for a respective

class processor which, in part, allows class processors to respond to selected data messages on host communication infrastructure and perform selected computations utilizing their respective read/write memory. Rather, Robinson '838 in view of Robinson '837 appear to describe a system where pre-partitioned object oriented processors respond to host processor messages broadcast across the common bus based upon bus addresses for each object oriented processor.

Further, Robinson '837 describes a memory management scheme for a block of contiguous memory, specifically RAM 14, and not class processors each having an associated private localized read/write memory as illustrated in Figure 1 of the present application. Robinson '838 describes pre-partitioned object oriented processors, sharing a common bus, which are configured to respond to specifically addressed messages from the host processor on the shared common bus.

For the reasons set forth above, Claim 1 is submitted to be patentable over Robinson '838 in view of Robinson '837.

The rejection of Claims 2-12 under 35 U.S.C. § 103 as being unpatentable over Robinson '838 in view of Robinson '837 and further in view of admitted prior art is respectfully traversed.

Claims 2-12 depend, directly or indirectly, from independent Claim 1 which is submitted as being patentable for the reasons given above. When the recitations of Claims 2-12 are considered in combination with the recitations of Claim 1, Applicants submit that dependent Claims 2-12 likewise are patentable over Robinson '838 in view of Robinson '837 and further in view of admitted prior art.

With respect to Claim 4, Robinson '838 in view of Robinson '837 and further in view of admitted prior art do not describe, nor suggest, a system wherein class processors are configured to reference other class processors through their respective application program interface modules. Rather, Robinson '838 in view of Robinson '837 and further in view of admitted prior art describe, referring specifically to Robinson '838 at Column 18, lines 10-30, providing another

object oriented processor with a periodic message generator, a link table, and linking scripts to enable direct communications between other object oriented processors.

Further, with respect to Claim 5, for example, Robinson '838 in view of Robinson '837 and further in view of admitted prior art do not describe, nor suggest, class processors which comprises a plurality of classes of class processors, at least one of which has an associated protected localized read/write memory accessible only to itself and class processors of the same class. Rather, and as described above, Robinson '838 in view of Robinson '837 and further in view of admitted prior art describe a memory management scheme for a block of contiguous memory, not localized read/write memory. In addition, Robinson '838 in view of Robinson '837 and further in view of admitted prior art do not describe nor suggest semi-private busses coupling class processors of the same class as recited in Claim 6. Still further, Robinson '838 in view of Robinson '837 and further in view of admitted prior art do not describe nor suggest class processors which include private localized read/write memory, protected localized read/write memory, and/or public localized read write memory as recited in Claims 7, 9, and 10. For these reasons, in addition to those given above, Applicants submit that dependent Claims 2-12 likewise are patentable over Robinson '838 in view of Robinson '837 and further in view of admitted prior art.

The rejection of Claim 13 under 35 U.S.C. § 103 as being unpatentable over Robinson '838 in view of Patel et al. (U.S. Patent No. 5,513,369) is respectfully traversed.

Robinson '838 is described above. Patel et al. describe subsystems each including a plurality of processors 14, each of which is linked to a star coupler device 20 by a cable 12. Cables 18 interconnect the star coupler devices of each subsystem. Each star coupler device 20 includes two star couplers 22 and 24. Star coupler 22 is connected via cables 12 with processors 14. Each cable includes a pair of conductors, one of which is connected to carry messages from the associated processor to the star coupler, while the second conductor conducts messages from the star coupler device to its associated processor. Within each subsystem, star coupler 22

operates in a conventional manner such that any message that is received by star coupler 22 from a linked processor 14 via cables 12 will be retransmitted to each of the linked processors, including the processor that generated the message.

Claim 13 recites a method for designing a distributed processing system for an application. The method comprises the steps of "partitioning the application into functions and data messages," "configuring a host processor having a host communication infrastructure (HCI) to pass data messages via the HCI to control the application," "configuring a plurality of class processors to compute the functions into which the application is partitioned in response to the data messages" and "interconnecting the class processors to the host processor via application program interface modules in a star configuration, the application program interface modules each defining a programming interface for one or more respective class processors."

Robinson '838 in view of Patel et al. do not describe, nor suggest the claimed method. Specifically, Robinson '838 in view of Patel et al. do not describe nor suggest configuring a plurality of class processors to compute the functions into which the application is partitioned in response to the data messages where application program interface modules each define a programming interface for one or more respective class processors. Rather, Robinson '838 describes pre-partitioned object oriented processors which are configured to respond to specifically addressed messages from the host processor. Patel et al. describe a system where each processor is directly connected to a host processor which manages and distributes the processing load amongst the other processors. Defining programming interfaces for individual class processors is not described nor suggested.

For the reasons set forth above, Claim 13 is submitted to be patentable over Robinson '838 in view of Patel et al.

The rejection of Claims 14 and 17-18 under 35 U.S.C. § 103 as being unpatentable over Robinson '838 in view of Patel et al. and further in view of Robinson '837 is respectfully traversed.

Claims 14 and 17-18 depend, directly or indirectly, from independent Claim 13 which is submitted as being patentable for the reasons given above. When the recitations of Claims 14 and 17-18 are considered in combination with the recitations of Claim 13, Applicants submit that dependent Claims 14 and 17-18 likewise are patentable over Robinson '838 in view of Patel et al. and further in view of Robinson '837.

Further, Robinson '838 in view of Patel et al. and further in view of Robinson '837 do not describe nor suggest a class processor having a private localized read/write memory as recited in Claim 14. Rather, a memory management scheme for a block of contiguous memory is described, specifically RAM 14, and not class processors each having an associated private localized read/write memory. Claims 17 and 18 depend from Claim 14. For these reasons, in addition to those given above, Applicants submit that dependent Claims 14, 17, and 18 are patentable over Robinson '838 in view of Patel et al. and further in view of Robinson '837.

The rejection of Claims 15 and 16 under 35 U.S.C. § 103 as being unpatentable over Robinson '838 in view of Robinson '837 and Patel et al. and further in view of admitted prior art is respectfully traversed.

Claims 15 and 16 depend, directly or indirectly, from independent Claim 13 which is submitted as being patentable for the reasons given above. When the recitations of Claims 15 and 16 are considered in combination with the recitations of Claim 13, Applicants submit that dependent Claims 15 and 16 likewise are patentable over Robinson '838 in view of Robinson '837 and Patel et al. and further in view of admitted prior art. Further, Robinson '838 in view of Robinson '837 and Patel et al. and further in view of admitted prior art do not describe nor suggest class processors comprising a protected read/write memory as recited in Claim 16.

The rejection of Claim 19 under 35 U.S.C. § 103 as being unpatentable over Robinson '838 in view of Patel et al. and further in view of admitted prior art is respectfully traversed.

Claim 19 depends from independent Claim 13 which is submitted as being patentable for the reasons given above. When the recitations of Claim 19 are considered in combination with the recitations of Claim 13, Applicants submit that dependent Claim 19 likewise is patentable over Robinson '838 in view of Patel et al. and further in view of admitted prior art.

In addition, Applicants respectfully submit that the Section 103 rejections of the presently pending claims are not proper rejections. As is well established, obviousness cannot be established by combining the teachings of the cited art to produce the claimed invention, absent some teaching, suggestion, or incentive supporting the combination. None of Robinson '838, Robinson '837, Patel et al. or the admitted prior art, considered alone or in combination, describe or suggest the claimed combination. Furthermore, in contrast to the assertion within the Office Action, Applicants respectfully submit that it would not be obvious to one skilled in the art to variously combine Robinson '838, Robinson '837, Patel et al. and the admitted prior art, because there is no motivation to combine the references suggested in the art. Additionally, the Examiner has not pointed to any prior art that teaches or suggests to combine the disclosures, other than Applicants' own teaching. Rather, only conclusory statements like "it would have been obvious to apply the teaching of the admitted prior art to the system of Robinson because it provides powerful computational platforms on a single chip" or "it would have been obvious to apply the teaching of Robinson '837 to the system of Robinson '838 because it provides an object oriented processor array that utilizes memory in an efficient manner" suggests combining the disclosures.

As the Federal Circuit has recognized, obviousness is not established merely by combining references having different individual elements of pending claims. Ex parte Levengood, 28 U.S.P.Q.2d 1300 (Bd. Pat. App. & Inter. 1993). MPEP 2143.01. Rather, there must be some suggestion, outside of Applicants' disclosure, in the prior art to combine such references, and a reasonable expectation of success must be both found in the prior art, and not based on Applicant's disclosure. In re Vaeck, 20 U.S.P.Q.2d 1436 (Fed. Cir. 1991). In the present case, neither a suggestion or motivation to combine the prior art disclosures, nor any reasonable expectation of success has been shown.

Furthermore, it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the cited art so that the claimed invention is rendered obvious. Specifically, one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the art to deprecate the claimed invention. Further, it is impermissible to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. The present Section 103 rejections are based on a combination of teachings selected from multiple patents in an attempt to arrive at the claimed invention. Specifically, Robinson '838 is cited for its teaching of a host processor communicating with object oriented processors, albeit not through application program interface modules each define a programming interface. Robinson '837 is cited for its teaching of memory management of contiguous memory, Patel et al. is cited for teaching star processing configurations, and the admitted prior art is cited merely for teaching single chip integrated circuit fabrication. Since there is no teaching nor suggestion in the cited art for the various combinations, the Section 103 rejections appear to be based on hindsight reconstruction in which isolated disclosures have been picked and chosen in an attempt to deprecate the present invention. Of course, such a combination is impermissible, and for this reason alone, Applicants request that the Section 103 rejections of Claims 1-19 be withdrawn.

In addition, as is well established, obviousness cannot be established by combining the teachings of the cited art to produce the claimed invention, absent some teaching, suggestion, or incentive supporting the combination. None of Robinson '838, Robinson '837, Patel et al. and the admitted prior art, considered alone or in combination, describe or suggest the distributed processing system and associated methods as recited in the claims. For these reasons, in addition to the reasons set forth above, Applicants request that the Section 103 rejections of Claims 1-19 be withdrawn.

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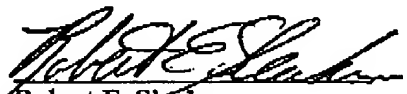
In view of the foregoing amendments and remarks, all the claims now active in this application are believed to be in condition for allowance. Reconsideration and favorable action is respectfully solicited.

Respectfully Submitted,



Robert E. Slenker
Registration No. 45,112
ARMSTRONG TEASDALE LLP
One Metropolitan Square, Suite 2600
St. Louis, Missouri 63102-2740
(314) 621-5070